

**CLAIMS**

**WHAT IS CLAIMED:**

1. A method, comprising:

providing an interconnect having a plurality of ports for communicating transactions  
5 between a plurality of domains in a computing system, the ports each being associated with a subset of the domains and the interconnect including a first signal path for transmitting a first portion of the transaction and a second signal path for transmitting a second portion of the transaction;  
identifying a transaction issued from one of ports associated with more than one of the domains;  
identifying an error in one of the first and second portions of the transaction; and canceling the transaction responsive to identifying the error.

2. The method of claim 1, wherein the first and second portions of the transaction

15 include control information and payload information, the control information for the first and second portions being the same, and the payload information for the first and second portions being different, and wherein identifying the error in the method further comprises identifying an error in the control information of the first and second portions.

20 3. The method of claim 1, wherein identifying the error further comprises performing a parity check.

4. The method of claim 1, wherein the first and second portions of the transaction each include control information, and identifying the error further comprises performing a parity check on the control information for the first and second portions.  
25

5        5.      The method of claim 1, wherein the interconnect further comprises a first arbiter associated with the first signal path and a second arbiter associated with the second signal path, and the method further comprises, responsive to identifying the error in one of the first and second portions of the transaction, sending a notification signal to the one of the first and second arbiters associated with the other of the first and second portions of the transaction.

10        6.      The method of claim 1, further comprising inhibiting future transactions from being issued from the port that originated the errant transaction.

15        7.      The method of claim 1, further comprising pausing the transaction prior to identifying the error.

20        8.      A method for communicating transactions, comprising:  
                  receiving a first portion of a transaction in a first device;  
                  receiving a second portion of the transaction in a second device in lockstep with respect to the first device;  
                  identifying an error in one of the first and second portions of the transaction; and  
                  notifying the device associated with the other of the first and second portions of the transaction responsive to identifying the error.

25        9.      The method of claim 8, further comprising canceling the transaction responsive to notifying the other device.

TUTORIAL - 6 PAGES OUT

10. The method of claim 8, wherein the first and second portions of the transaction include control information and payload information, the control information for the first and second portions being the same, and the payload information for the first and second portions being different, and wherein identifying the error in the method further comprises identifying  
5 an error in the control information of the first and second portions.

11. The method of claim 8, wherein identifying the error further comprises performing a parity check.

10. The method of claim 8, wherein the first and second portions of the transaction each include control information, and identifying the error further comprises performing a parity check on the control information for the first and second portions.

13. The method of claim 8, further comprising:

15 providing a port for issuing the transaction to the first and second devices; and inhibiting future transactions from being issued from the port that originated the transaction responsive to the notification signal.

14. The method of claim 8, further comprising pausing the transaction in the first  
20 and second devices prior to identifying the error.

15. A computing system, comprising:

a plurality of system domains;  
an interconnect having a plurality of ports for communicating between the system  
25 domains, the interconnect including a first signal path for transmitting a first

portion of a transaction and a second signal path for transmitting a second portion of the transaction;

a first arbiter associated with the first signal path and being configured to identify a transaction issued from a port associated with more than one of the domains and detect an error in the first portion of the transaction; and

5 a second arbiter associated with the second signal path and being configured to identify an error in the second portion of the transaction issued from the port associated with more than one of the domains;

wherein the first and second arbiters are adapted to cancel the transaction responsive to identifying the error in either of the first and second portions of the transaction.

16. The system of claim 15, wherein the first and second portions of the transaction include control information and payload information, the control information for the first and second portions being the same, and the payload information for the first and second portions being different, and wherein the first and second arbiters are configured to identify errors in the control information of the first and second portions, respectively.

17. The system of claim 15, wherein the first and second arbiters are configured to perform a parity check.

20 25 18. The system of claim 15, wherein the first and second portions of the transaction each include control information, and the first and second arbiters are configured to perform a parity check on the control information for the first and second portions.

19. The system of claim 15, wherein one of the first and second arbiters, responsive to identifying the error in one of the first and second portions of the transaction, is further configured to send a notification signal to the other of the first and second arbiters.

5        20. The system of claim 15, wherein the first and second arbiters are further configured to inhibit future transactions from being issued from the port that originated the errant transaction.

10        21. The system of claim 15, wherein the first and second arbiters are adapted to pause the transaction issued from the port associated with more than one of the domains prior to identifying the errors.

15        22. A computing system for communicating transactions, comprising:  
a first device adapted to receive a first portion of a transaction; and  
a second device adapted to receive a second portion of the transaction in lockstep with  
respect to the first device, wherein the first and second devices are further  
configured to identify an error in one of the first and second portions of the  
transaction, respectively, and the one of the first and second devices that  
identifies the error is further configured to send a notification signal to the  
device associated with the other of the first and second portions of the  
20 transaction responsive to identifying the error.

23. The system of claim 22, wherein the first and second devices are further  
configured to cancel the transaction responsive to the notification signal.

TOKYO/TOKYO/10003490-1010104

15

20

25

24. The system of claim 22, wherein the first and second portions of the transaction include control information and payload information, the control information for the first and second portions being the same, and the payload information for the first and second portions being different, and the first and second devices are further configured to identify the error in the control information of the first and second portions, respectively.

5  
25. The system of claim 22, wherein the first and second devices are further configured to perform a parity check on the first and second portions, respectively.

10  
26. The system of claim 22, wherein the first and second portions of the transaction each include control information, and the first and second devices are further configured to identify the error by performing a parity check on the control information for the first and second portions, respectively.

15  
27. The system of claim 22, wherein the first and second devices are adapted to pause the transaction prior to identifying the error.

20  
28. A computing system, comprising:  
a first system domain;  
a second system domain; and  
an interconnect between the first and second system domains, the interconnect comprising two halves, each half transmitting a portion of a transaction between the first and second domains, and being configured to error check the two portions and cancel the transaction if an error is identified.

29. The system of claim 28, wherein the transaction includes control information and payload information, the control information for the portion associated with the first half and the portion associated with the second half being the same, and the payload information for the portion associated with the first half and the portion associated with the second half being different, and wherein the interconnect is configured to identify errors in the control information of the portions.

30. The system of claim 28, wherein the interconnect is configured to perform a parity check on the portions.

31. The system of claim 28, wherein the transaction includes control information, and the interconnect is configured to perform a parity check on the control information for the portion associated with the first half and the portion associated with the second half.

32. The system of claim 28, wherein one of the first and second halves, responsive to identifying the error, is further configured to notify the other half.

33. The system of claim 28, wherein the interconnection includes at least one port for originating the transaction, and the first and second halves are further configured to inhibit future transactions from being issued from the port that originated the transaction.

34. The system of claim 28, wherein the interconnect is adapted to pause the transaction prior to identifying the errors.

35. A system, comprising:

means for communicating transactions between a plurality of domains in a computing

system including first means for transmitting a first portion of the transaction

and second means for transmitting a second portion of the transaction;

5

means for identifying an error in one of the first and second portions of the  
transaction; and

means for canceling the transaction responsive to identifying the error.

10034610-140101

16  
36. A system, comprising:

means for receiving a first portion of a transaction;

means for receiving a second portion of the transaction in lockstep with respect to the

means for receiving the first portion;

means for identifying an error in one of the first and second portions of the  
transaction; and

15  
means for sending a notification signal to the means associated with the other of the

first and second portions of the transaction responsive to identifying the error.